REMARKS

The enclosed is responsive to the Examiner's Final Office Action mailed on August 22, 2008. At the time the Examiner mailed the Final Office Action claims 1, 2, 5-8, 10-19, 21-26, 28 and 29 were pending. By way of the present response the Applicants have: 1) amended claims 1, 18, 18 and 24; 2) added no new claims; and 3) canceled claims 10-17. As such, claims 1, 2, 5-7, 18, 19, 21-26, 28 and 29 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims now represented.

Specification

The Office Action states that "[a]s admitted by applicant, and now according to at least amended claim 1, the three debug register fields are a part of the processor control register. As previously discussed, these fields are not added or attached to the control status register. Hence, applicant is requested to locate all portions of the specification (not the claims) which discuss adding/attaching these fields and change the language appropriately." Applicants do not understand what the Office Action is getting at. First, the claim requires that "at least three degug register bits fields of at least one processor control status register" are "manipulate[d]" and not that they are added or attached to the processor control status register. Second, while claim 1 does use the word "attaches" it is referring to the attachment of "at least one breakpoint bit field...directly to one or more instructions...," but not in conjunction with the processor control register. Accordingly, Applicants respectfully submit that it is unnecessary to either amend the claim or provide support for a claim limitation that does not exist.

Claim Objections

Claim 1 was objected to because of informalities. While Applicants do not believe that any correction is required, Applicants have amended the claim

in a manner consistent with what the Office Action requested. No new matter has been added by these non-narrowing amendments.

Claim 18 is objected to because of informalities. While Applicants do not believe that any correction is required, Applicants have amended the claim in a manner consistent with what the Office Action requested. No new matter has been added by these non-narrowing amendments.

Claim 19 is objected to because of informalities. While Applicants do not believe that any correction is required, Applicants have amended the claim in a manner consistent with what the Office Action requested. No new matter has been added by these non-narrowing amendments.

Claim 24 is objected to because of informalities. While Applicants do not believe that any correction is required, Applicants have amended the claim in a manner consistent with what the Office Action requested. No new matter has been added by these non-narrowing amendments.

Claim Rejections

35 U.S.C. 103(a) Rejections

The Office Action rejected claims 1-2, 5-8, 18-19, 21-26 and 28-29 under 35 U.S.C. 103(a) as being unpatentable over Glew, et al., U.S. Patent 5,694,589 (hereinafter "Glew") in view of IBM Technical Disclosure Bulletin NN8907370 (as previously cited and herein referred to as "IBM"), and further in view of Deng, et al., U.S. Patent 6,951,416 (hereinafter "Deng").

Glew discloses code breakpoint detection logic for a superscalar microprocessor. (Glew at Abstract.) IBM discloses a technique that provides a breakpoint function in a processor without the use of extra comparison logic and with minimal delay. (IBM at Disclosure Text.) Deng discloses debugger circuitry that is implemented on the microcontroller itself and that may break application program execution upon detection of a specified condition, display internal register values to the user, and continue the application program execution. (Deng at col. 2, ll. 37-41.)

The combination of Glew, IBM, and Deng does not describe what Applicants' claims require. With respect to claim 1, the combination does not describe:

> An apparatus comprising:
> a memory;
> a plurality of processors coupled to the memory; and
> a controller coupled to the memory and the plurality of processors, the controller to execute a debug process that:
> attaches at least one breakpoint bit field comprising a single bit directly to one or more instructions of the plurality of processors, each breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of an instruction of the one or more instructions to which breakpoint bit field is attached without having to perform an address comparison;
> manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprising a run field, a single step field, and a debug enable field that each comprise a single bit; and
> accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM (LDTI) instruction and a Load from Instruction RAM (LDFI) instruction.

Specifically, Applicants submit that the combination does not at least describe a debug process that "manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprising ***a run field, a single step field, and a debug enable field that each comprise a single bit***." The Office Action cites Deng as allegedly describing this feature. Deng's Figure 16 ("breakpoint control register") includes four bits (BE1-BE4) which "contain the four address breakpoint enables," a single step enable bit, and a global debugger enable bit amongst other bits (two bits for a stack pointer comparison function). (*See* Deng, col.9 ll.21-26 and Fig. 16.)

None of these is a single-bit run field. While the Office Action equates any one of the BE bits as the run field of claim 1, such a reading of eliminating the other three BE bits would render Deng as being "unsatisfactory for its intended purpose" and thus there would be "no suggestion or motivation" to make such a change to Deng. (*See* MPEP 2143.01.) Deng must be considered in its entirety, as required by MPEP 2141.02 and 2141, and Deng requires that each of the BE bits be used. For example, each of the BE bits are used in Fig. 2 when "[a]ddress breakpoint circuitry" compares four address breakpoint signals ("AD") with their respective breakpoint enable singles ("BE"). (*See* Deng, col.5 ll.47-53 and Fig. 2.) Moreover, in order to be useful the BE bits clearly requires the use of a other bits, ADs, to be of any use whatsoever. (*Id.*) As such, a single BE bit cannot and does not describe Applicants claimed "run field." Additionally, neither Glew nor IBM describe this limitation.

Moreover, at least Deng and IBM are uncombinable. As discussed above, Deng requires the comparison of a plurality of address bits (AD) with breakpoint enable bits (BE). IBM "describes a technique which provides a breakpoint function in a processor without the use of extra comparison logic...[which would] periodically compare" a breakpoint register with an address." (IBM, emphasis added.) Thus, IBM teaches away from the combination of Glew, IBM, and Deng.

Thus, the combination of Glew, IBM, and Deng does not describe what Applicants' claim 1 requires. Claims 2 and 5-8 are ultimately dependent on claim 1 and are allowable for at least the same reason.

Independent claims 18 and 24 also recite the above-cited feature of claim 1. As a result, claims 18 and 24, as well as their respective dependent claims, are also patentable over the combination of Glew, IBM, and Deng.

In light of the comments above, the Applicants respectfully request the allowance of all claims.

CONCLUSION

Applicants respectfully submit that all rejections have been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact David F. Nicholson at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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/David F. Nicholson/
David F. Nicholson
Reg. No.: 62,888

1279 Oakmead Parkway
Sunnyvale, CA 94085
(408) 720-8300